

In re Patent Application of  
**GARNIER ET AL.**  
Serial No. 09/499,060  
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*cont'd*  
*Sub E1*

proportional to a square of a ratio of the second resistance and the first resistance.

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In re Patent Application of  
**GARNIER ET AL.**  
Serial No. 09/499,060  
Filed: February 4, 2000

said current generator is based upon the equation:

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$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity  $k \frac{T}{q}$ , where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

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15. (Twice Amended) An integrated circuit voltage ramp generator comprising:

a semiconductor substrate;

a capacitance on said semiconductor substrate; and

a charging circuit on said semiconductor substrate and connected to said capacitance and comprising

a current generator having a first resistance, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance.

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17. (Amended) An integrated circuit voltage ramp generator according to Claim 15, wherein said degenerate

In re Patent Application of  
**GARNIER ET AL.**  
Serial No. 09/499,060  
Filed: February 4, 2000

current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

cont'd  
a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

18. (Amended) An integrated circuit voltage ramp generator according to Claim 17, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

19. (Amended) An integrated circuit voltage ramp generator according to Claim 15, wherein said capacitance comprises a gate capacitance of a MOS transistor.

20. (Amended) An integrated circuit voltage ramp generator according to Claim 15, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a

In re Patent Application of  
**GARNIER ET AL.**  
Serial No. 09/499,060  
Filed: February 4, 2000

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reference voltage proportional to the quantity  $k \frac{T}{q}$ , where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

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21. (Twice Amended) An integrated circuit current ramp generator comprising:

a semiconductor substrate;  
a voltage ramp generator on said semiconductor substrate and comprising  
a capacitance, and  
a charging circuit connected to said capacitance and comprising  
a current generator having a first resistance, and  
a circuit connected to said current generator and to said capacitance having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and  
a conversion circuit on said semiconductor substrate and connected to said voltage ramp generator for generating a current ramp.

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22. (Amended) An integrated circuit current ramp generator according to Claim 21, wherein said conversion circuit comprises a third resistance.

23. (Amended) An integrated circuit current ramp generator according to Claim 21, wherein said third resistance

In re Patent Application of  
**GARNIER ET AL.**  
Serial No. 09/499,060  
Filed: **February 4, 2000**

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comprises an implanted resistance having a positive temperature coefficient.

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24. (Amended) An integrated circuit current ramp generator according to Claim 21, wherein said charging circuit comprises a degenerate current mirror circuit on said semiconductor substrate.

25. (Amended) An integrated circuit current ramp generator according to Claim 24, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

26. (Amended) An integrated circuit current ramp generator according to Claim 25, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

27. (Amended) An integrated circuit current ramp generator according to Claim 21, wherein said capacitance comprises a gate capacitance of a MOS transistor.

28. (Amended) An integrated circuit current ramp

In re Patent Application of  
**GARNIER ET AL.**  
Serial No. 09/499,060  
Filed: February 4, 2000

generator according to Claim 21, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity  $k\frac{T}{q}$ , where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

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29. (Twice Amended) An integrated circuit current ramp generator comprising:

a semiconductor substrate;  
a voltage ramp generator on said semiconductor substrate and comprising  
a capacitance having a first resistance, and  
a charging circuit connected to said capacitance and comprising  
a current generator, and  
a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance; and

In re Patent Application of  
**GARNIER ET AL.**  
Serial No. 09/499,060  
Filed: February 4, 2000

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a third resistance on said semiconductor substrate  
and connected to said voltage ramp generator for generating a  
current ramp.

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31. (Amended) An integrated circuit current ramp generator according to Claim 29, wherein said third resistance comprises an implanted resistance having a positive temperature coefficient.

32. (Amended) An integrated circuit current ramp generator according to Claim 29, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

33. (Amended) An integrated circuit current ramp generator according to Claim 32, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

34. (Amended) An integrated circuit current ramp generator according to Claim 29, wherein said capacitance comprises a gate capacitance of a MOS transistor.

In re Patent Application of  
**GARNIER ET AL.**  
Serial No. 09/499,060  
Filed: February 4, 2000

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35. (Amended) An integrated circuit current ramp generator according to Claim 29, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where  $Ig2$  is the current,  $K2$  is a proportionality coefficient,  $Rg2$  is the first resistance, and  $Vg2$  is a reference voltage proportional to the quantity  $k \frac{T}{q}$ , where  $k$  is the Boltzmann constant,  $T$  is absolute temperature, and  $q$  is the charge of an electron.

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36. (Twice Amended) A method for generating a ramp voltage comprising:

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generating a capacitance charging current using an integrated circuit charging circuit comprising a semiconductor substrate, and a current generator on the semiconductor substrate and having a first resistance and a circuit on the semiconductor substrate and connected to the generator having a second resistance for enabling the capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

*Sub 1*

charging a capacitance on the semiconductor substrate with the capacitance charging current for generating the ramp voltage.

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37. (Amended) A method according to Claim 36, wherein the circuit comprises a degenerate current mirror